Docket No.: 50090-265

PATENT

#5/Elect.
4/26/02
Hays

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
Kiyotoshi UEDA, et al.	:	
Serial No.: 09/766,845	:	Group Art Unit: 2829
Filed: January 23, 2001	:	Examiner: P. Patel

For: METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT MANUFACTURED THEREBY

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
Washington, DC 20231

Sir:

Noting the Office Action of March 11, 2002 wherein restriction has been required, Applicant(s) hereby elect Species 1 of Fig. 4 (claims 1-11 and 13-14 being readable thereon) for prosecution in the above-identified application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Stephen A. Becker
Registration No. 26,527

600 13th Street, N.W.
Washington, DC 20005-3096
(202)756-8000 SAB:cms
Facsimile: (202)756-8087
Date: April 11, 2002